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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,161	10/31/2003	Yu-Chih Wang	252011-1770	9843

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EXAMINER	
JARRETT, RYAN A	
ART UNIT	**PAPER NUMBER**
2125	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,161	WANG ET AL.	
	Examiner	Art Unit	
	Ryan A. Jarrett	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/15/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9,12-17,20-24 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,12-17,20-24 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. Claims 1, 4-9, 12-17, 20-24, and 33 are presented for examination.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/13/05 has been entered.

Response to Arguments

3. Applicant argues that Goerigk does not teach the features of the new limitation added to independent claims 1, 9, 17, and 33 in the amendment filed 6/15/05. This amendment has been rejected under 35 USC 112, 1st paragraph and 2nd paragraph, as discussed below. Since there is no explicit or implicit disclosure of this new limitation in the original disclosure, this new limitation is being broadly interpreted in light of the specification on page 8 line 24 – page 9 line 4.

On page 8 line 24 – page 9 line 4 of the Applicant's specification, it is disclosed, "A data verification procedure is executed according to a MES database after the first process operation 40. A verification result is then obtained by the verification

procedure. The data verification procedure verifies the data between the actual wafers and the MES database. If a carrier transfer sub-route is required according to the verification result, a carrier transfer sub-route is then produced and executed". So, the specification discloses that the sub-route is generated based only on the verification result. The verification result indicates whether a carrier transfer sub-route is required. This is how the claim limitation is being interpreted. There is no disclosure of "correlating" process operation information with carrier transfer operation information in order to generate the carrier transfer sub-route; according to the original specification, the sub-route is generated based only on the verification result.

Goerigk teaches this broad interpretation. In col. 9 lines 2-9, Goerigk discloses, "Accordingly, wafers in the production line may be resorted in accordance with process requirements, or one or more wafers may be split off or merged to the lot. The control unit may also update the unique wafer position information of the wafer on the basis of attribute information stored in the memory unit and regroups the wafers so as to achieve minimum retention time of the wafer in the production line." Since the wafers of Goerigk are regrouped based on attribute information stored in the database memory, this corresponds to generating a sub-route based on a database verification result, as claimed by the Applicant.

If the limitation is construed more narrowly, Goerigk still teaches the feature, as best understood (e.g., col. 6 line 55 – col. 7 line 12, col. 8 lines 1-24, col. 8 line 66 – col. 9 line 20). In col. 8 lines 1-24, Goerigk discloses, "the position of the wafer may be changed in accordance with process requirements, wherein the unique position

information is brought into conformity with the new current position of the wafer". Thus, the original wafer position information of Goerigk (stored in the database memory as wafer attribute information) corresponds to the "carrier transfer operations information" of Applicant's claims, and the "process requirement" of Goerigk (also stored in the database memory as wafer attribute information) corresponds to the "process operation information" of the Applicant's claims. The original wafer position of Goerigk is changed, or updated in accordance with the process requirements, wherein the changing is performed by a wafer sorter. This changing of the wafer position by the wafer sorter of Goerigk corresponds to the "carrier transfer sub-route" of the Applicant's claims. And since the original wafer position is changed "in accordance" with the process requirements in Goerigk, this corresponds to the "correlating" step of Applicant's claims.

Regarding claims 8, 16, and 24, Applicant states that the previous Office Action does not indicate any teaching or suggestion of the prior art for the limitation recited in these claims. A reference (Sada et al.) has been applied by the Examiner to reject this feature under 35 U.S.C. 103. Since Sada et al. can also be used to reject these claims under 35 U.S.C 102, the reference has been applied in a separate rejection to reject claims 1, 7-9, 15-17, 23, 24, and 33 under 35 U.S.C. 102(b).

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 9 and 12-16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are directed to "a storage medium for storing a computer program". This "storage medium" may be interpreted to be a piece of paper with a computer program written on it (i.e., which is not computer-readable) which, through the intermediary of a scanner could supply the program to execute on a computer for performing the claimed steps. As such, this is not a statutory manufacture under 35 U.S.C. 101.

The "storage medium" should be amended to "computer-readable storage medium".

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1, 4-9, 12-17, 20-24, and 33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding independent claims 1, 9, 17, and 33, Examiner has been unable to find explicit or implicit support for the new limitation added in the amendment filed 5/13/05: "dynamically producing a carrier transfer sub-route of the wafers according to

the verification result by accessing first information corresponding to process operations and second information corresponding to carrier transfer operations and then correlating the first information and the second information to generate the carrier transfer sub-route". If applicant believes that this new limitation is implied or inherent based on the original disclosure, then applicant is requested to specifically point out the portion of the specification that makes this new limitation implied or inherent.

Claims 4-9, 12-17, and 20-24 depend from claims 1, 9, and 17, and thus incorporate the same deficiencies.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1, 4-9, 12-17, 20-24, and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding independent claims 1, 9, 17, and 33, Examiner has been unable to find explicit or implicit support for the new limitation added in the amendment filed 6/15/05: "dynamically producing a carrier transfer sub-route of the wafers according to the verification result by accessing first information corresponding to process operations and second information corresponding to carrier transfer operations and then correlating the first information and the second information to generate the carrier transfer sub-route". This limitation has been rejected under 35 U.S.C. 112, second paragraph, for the following reason:

It is not clear how the "carrier transfer operations" differ from the "carrier transfer sub-route". The specification defines "carrier transfer operations" to be carrier sort and merge operations (e.g., pg. 1 lines 18-20). The specification defines "carrier transfer sub-route" to be a transferring of wafers in one carrier to different carriers, or a splitting of wafer in one carrier and then transferring the split lots to different carriers (e.g., page 3 lines 3-6). Thus, "carrier transfer operations" and "carrier transfer sub-route" both relate to the transferring, splitting, sorting, and/or merging of wafers between different carriers. Based on the Applicant's specification, the two terms appear to be referring to essentially the same type of operation. However, the language of the claim implies that these are two different types of operations, or two different types of data, by reciting that the carrier transfer sub-route is generated based in part on the carrier transfer operations. It is not clear how these two terms differ.

As best understood, the claim is being interpreted in light of the specification on page 8 line 24 – page 9 line 4. Here, it is disclosed, "A data verification procedure is executed according to a MES database after the first process operation 40. A verification result is then obtained by the verification procedure. The data verification procedure verifies the data between the actual wafers and the MES database. If a carrier transfer sub-route is required according to the verification result, a carrier transfer sub-route is then produced and executed". So, the specification discloses that the sub-route is generated based only on the verification result. The verification result indicates whether a carrier transfer sub-route is required. This is how the claim limitation is being interpreted. There is no disclosure of "correlating" process operation

information with carrier transfer operation information in order to generate the carrier transfer sub-route; the sub-route is generated based only on the verification result.

Claims 4-9, 12-17, and 20-24 depend from claims 1, 9, and 17, and thus incorporate the same deficiencies.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. As best understood, claims 1, 4-5, 7, 9, 12-13, 15, 17, 20-21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Goerigk U.S. Patent No. 6,303,398. Goerigk discloses:

1. A computer-implemented method of automatic carrier transfer, comprising using a computer to perform the steps of:

executing a data verification procedure after a first process operation of a plurality of wafers according to a manufacturing execution system database and obtaining a verification result (e.g., col. 4 lines 44-54, col. 7 lines 13-24, col. 7 lines 43-50), wherein the data verification procedure verifies the data between the wafers and the MES database (col. 4 line 4 – line 5 line 18, col. 8 lines 57-65);

dynamically producing a carrier transfer sub-route of the wafers according to the verification result (e.g., col. 5 lines 19-38, col. 8 lines 1-24, col. 8 line 66 – col. 9 line 20) by accessing first information corresponding to process operations and second information corresponding to carrier transfer operations and then correlating the first information and the second information to generate the carrier transfer sub-route (e.g., col. 6 line 55 – col. 7 line 12, col. 8 lines 1-24, col. 8 line 66 – col. 9 line 20);

executing the carrier transfer sub-route of the wafers (e.g., col. 5 lines 19-38); and

executing a second process operation for the wafers (e.g., col. 5 lines 38-45).

4. The computer-implemented method of claim 1, wherein executing the carrier transfer sub-route further comprises updating the MES database (e.g., col. 5 line 45 – col. 6 line 18).

5. The computer-implemented method of claim 1, wherein the carrier transfer sub-route is enabled by transferring the wafers from a first carrier to a second carrier (e.g., col. 5 line 45 – col. 6 line 18).

7. The computer-implemented method of claim 1, wherein the first process operation and the second process operation are stored in a first database (e.g., col. 7 lines 43-55).

9. A storage medium for storing a computer program providing a method of automatic carrier transfer, comprising using a computer to perform the steps of:

executing a data verification procedure after a first process operation of a plurality of wafers according to a manufacturing execution system database and obtaining a verification result (e.g., col. 4 lines 44-54, col. 7 lines 13-24, col. 7 lines 43-50), wherein the data verification procedure verifies the data between the wafers and the MES database (col. 4 line 4 – line 5 line 18, col. 8 lines 57-65);

dynamically producing a carrier transfer sub-route of the wafers according to the verification result (e.g., col. 5 lines 19-38, col. 8 lines 1-24, col. 8 line 66 – col. 9 line 20) by accessing first information corresponding to process operations and second information corresponding to carrier transfer operations and then correlating the first information and the second information to generate the carrier transfer sub-route (e.g., col. 6 line 55 – col. 7 line 12, col. 8 lines 1-24, col. 8 line 66 – col. 9 line 20);

executing the carrier transfer sub-route of the wafers (e.g., col. 5 lines 19-38); and

executing a second process operation for the wafers (e.g., col. 5 lines 38-45).

12. The storage medium as claimed in claim 9, wherein executing the carrier transfer sub-route further comprises updating the MES database (e.g., col. 5 line 45 – col. 6 line 18).

13. The storage medium as claimed in claim 9, wherein the carrier transfer sub-route is enabled by transferring the wafers from a first carrier to a second carrier (e.g., col. 5 line 45 – col. 6 line 18).

15. The storage medium as claimed in claim 9, wherein the first process operation and the second process operation are stored in a first database (e.g., col. 7 lines 43-55).

17. A system for automatic carrier transfer, comprising:

a first execution module (e.g., Fig. 1 #5), executing a data verification procedure after a first process operation (e.g., Fig. 1 #6-9) of a plurality of wafers according to a manufacturing execution system database (e.g., Fig. 1 #2) and obtaining a verification result (e.g., e.g., col. 4 lines 44-54, col. 7 lines 13-24, col. 7 lines 43-50), wherein the data verification procedure verifies the data between the wafers and the MES database (col. 4 line 4 – line 5 line 18, col. 8 lines 57-65);

a sub-route production module (e.g., Fig. 1 #1), coupled to the first execution module, producing a carrier transfer sub-route according to the verification result (e.g., col. 5 lines 19-38, col. 8 lines 1-24, col. 8 line 66 – col. 9 line 20) by accessing first information corresponding to process operations and second information corresponding to carrier transfer operations and then correlating the first information and the second information to generate the carrier transfer sub-route (e.g., col. 6 line 55 – col. 7 line 12, col. 8 lines 1-24, col. 8 line 66 – col. 9 line 20);

a sub-route execution module (e.g., Fig. 1 #5), coupled to the sub-route production module, executing the carrier transfer sub-route of the wafers (e.g., e.g., col. 5 lines 19-38); and

a second execution module (e.g., Fig. 1 #6-9), coupled to the sub-route execution module, executing a second process operation for the wafers (e.g., col. 5 lines 38-45).

20. The apparatus as claimed in claim 17, wherein the sub-route execution module further updates the MES database (e.g., col. 5 line 45 – col. 6 line 18).

21. The apparatus as claimed in claim 17, wherein the carrier transfer sub-route is enabled by transferring the wafers from a first carrier to a second carrier (e.g., col. 5 line 45 – col. 6 line 18).

23. The apparatus as claimed in claim 17, wherein the first process operation and the second process operation are stored in a first database (e.g., col. 7 lines 43-55).

12. As best understood, claims 1, 7-9, 15-17, 23, 24, and 33 are additionally rejected under 35 U.S.C. 102(b) as being anticipated by Sada et al. U.S. Patent No. 6,174,375. Claims 9, 15-17, 23, and 24 are directed to a storage medium and a system, and are substantially the same as the computer-implemented method claims 1, 7, and 8, and are thus rejected for the same reasons. The claimed "database" is broadly interpreted to be a "large collection of data", or a memory as disclosed in Sada et al. Sada et al. discloses:

1. A computer-implemented method of automatic carrier transfer, comprising using a computer to perform the steps of:

executing a data verification procedure after a first process operation of a plurality of wafers according to a manufacturing execution system database and obtaining a verification result (e.g., col. 3 lines 22-36), wherein the data verification procedure verifies the data between the wafers and the MES database (e.g., col. 3 lines 22-36);

dynamically producing a carrier transfer sub-route of the wafers according to the verification result by accessing first information corresponding to process operations (e.g., col. 3 lines 22-36: *"lot status memory **4**"*) and second information corresponding to carrier transfer operations (e.g., col. 3 lines 37-59: *"branch content memory **5**"*) and then correlating the first information and the second information to generate the carrier transfer sub-route (e.g., col. 3 line 22 – col. 4 line 3);

executing the carrier transfer sub-route of the wafers (e.g., col. 3 lines 60-62); and

executing a second process operation for the wafers (e.g., col. 4 line 62 – col. 5 line 3).

7. The computer-implemented method of claim 1, wherein the first process operation and the second process operation are stored in a first database (e.g., col. 3 lines 22-36: *"lot status memory **4**"*).

8. The computer-implemented method as claimed in claim 7, wherein the carrier transfer sub-route is stored in a second database (e.g., col. 3 lines 37-50: *"branch content memory **5**"*).

33. A computer-implemented method of automatic carrier transfer, comprising using a computer to perform the steps of:

executing a data verification procedure after a first process operation of wafers according to a manufacturing execution system database and obtaining a verification result, (e.g., col. 3 lines 22-36), the data verification procedure verifying data between the wafers and the MES database (e.g., col. 3 lines 22-36);

dynamically selecting a carrier transfer sub-route of the wafers according to the verification result (e.g., col. 3 lines 37-59);

executing the carrier transfer sub-route of the wafers (e.g., col. 3 lines 60-62); and

executing a second process operation for the wafers (e.g., col. 4 line 62 – col. 5 line 3);

wherein the first process operation and the second process operation are stored in a first database and are selected for processing of the wafers prior to executing the first process operation (e.g., col. 3 lines 22-36: *"lot status memory **4**"*);

wherein the carrier transfer sub-route is stored in a second database (e.g., col. 3 lines 37-59: *"branch content memory **5**"*); and

wherein the carrier transfer sub-route is dynamically generated by accessing first information corresponding to process operations (e.g., col. 3 lines 22-36: *"lot status memory **4**"*) and second information corresponding to carrier transfer operations (e.g., col. 3 lines 37-59: *"branch content memory **5**"*) and then correlating the first information and the second information to generate the carrier transfer sub-route (e.g., col. 3 line 22 – col. 4 line 3).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 6, 14, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goerigk as applied to claims 1, 9, and 17 above, and further in view of Babbs et al. 6,520,727.

Goerigk discloses that the carrier transfer sub-route is enabled by transferring the wafers from a first carrier to a second carrier (e.g., col. 5 line 45 – col. 6 line 18).

Goerigk does not appear to explicitly disclose that the carrier transfer sub-route is enabled by transferring the split lots in the first carrier to at least two carriers.

However, Babbs et al. discloses a modular wafer sorter that splits wafers from one cassette into two or three other cassettes (col. 2 lines 29-40).

Goerigk and Babbs et al. are analogous art since they both pertain to sorting and splitting wafers into different cassettes.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Goerigk with Babbs since Babbs teaches that occasionally, semiconductor processing operations require three-wide sorter units and four-wide sorter units, for example where it is desired to split wafers from one cassette into two or three other cassettes (col. 2 lines 29-40). This teaching of Babbs would enable the routing of the split wafers of Goerigk to two different subsequent processes via two different carriers or cassettes.

15. Claims 8, 16, 24, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goerigk as applied to claims 7, 15, and 23 above, and further in view of Sada et al. U.S. Patent No. 6,174,375.

Goerigk discloses most all of the features of claim 33 as discussed above with respect to claim 1. Additionally, per claim 33, Goerigk discloses that the first process operation and the second process operation are stored in a database and are selected for processing of the wafers prior to executing the first process operation (e.g., col. 7 lines 51-55). The process operation information is a part of the wafer "attribute information" and it is stored in the memory unit, or database (e.g., Fig. 1 #2, col. 3 lines 62-66, col. 7 lines 43-55). Goerigk also discloses that the carrier transfer sub-route is stored in a database (e.g., col. 5 lines 49-54, col. 8 lines 1-24). This carrier transfer sub-route corresponds to the "wafer position information" of Goerigk, which comprises the wafer slot number and the cassette identifier. This wafer position information is also a part of the wafer "attribute information", and it is stored in the same memory unit, or database (e.g., Fig. 1 #2, col. 3 line 62-66, col. 7 lines 43-55).

Goerigk does not appear to *explicitly* disclose that the memory unit or database can be two separate databases.

However, Sada et al. discloses a semiconductor device manufacturing system capable of automatic branching and merging of wafers, including a first memory or database for storing the status of lots of semiconductor wafers, and a second memory or database for storing branch information of the lots of semiconductor wafers (e.g., col. 3 lines 22-27).

Goerigk and Sada et al. are analogous art since they both pertain to branching and merging wafers into different cassettes.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to separate the wafer attribute database of Goerigk into two databases: a process database and a carrier transfer sub-route database, as taught by Sada et al., in order to shorten the access time of the data managing system of Goerigk that selectively accesses the database (col. 3 lines 62-66 of Goerigk). Sada et al. determines whether or not wafers should be branched by accessing the lot status memory, or database. ***Only*** if it is determined that the wafers should be branched does the control of Sada et al. access the branch content memory (col. 3 lines 30-50 of Sada et al.). Thus, Sada et al. accesses a first database containing one set of information, and *only* accesses the second database containing a second set of information when necessary. The two smaller databases, as taught by Sada et al., would result in a smaller amount of stored data than that contained in the single larger database of Goerigk and would thus reduce the access time required when the computer program that controls the operation of the entire production line (col. 5 lines 25-27 of Goerigk) only needs to access one of the data sets. A single, larger database would require a longer access time. Sada et al. teaches the advantages of using two separate databases to store the process information and the carrier transfer sub-route information.

Conclusion

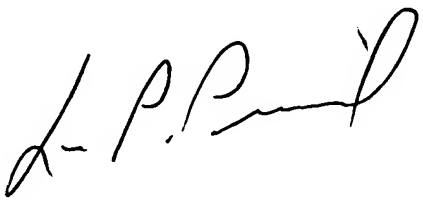
16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan A. Jarrett whose telephone number is (571) 272-3742. The examiner can normally be reached on 10:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Jarrett
Examiner
Art Unit 2125

RAJ
7/11/05



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TECHNOLOGY CENTER 2100